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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04N 7/01

A1

(11) International Publication Number: WO 99/34597

(43) International Publication Date: 8 July 1999 (08.07.99)

(21) International Application Number: PCT/US98/27542

(22) International Filing Date: 31 December 1998 (31.12.98)

(30) Priority Data:
09/001,596 31 December 1997 (31.12.97) US

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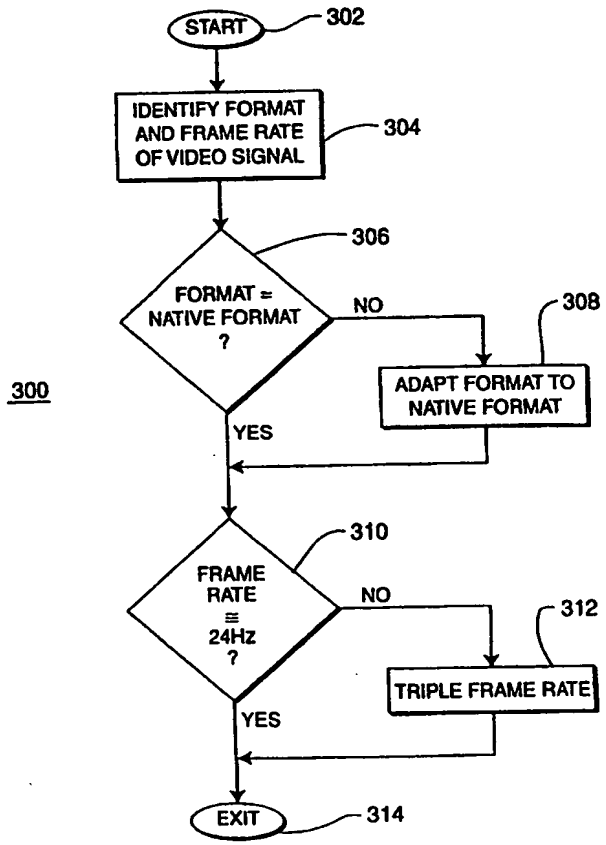
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: FORMAT AND FRAME RATE COMVERSION FOR DISPLAY OF 24 HZ SOURCE VIDEO

(57) Abstract

An apparatus for electronic format and frame rate conversion in a multiple format video processing system adapted to avoid display motion artifacts causes by 3:2 video source by tripling the frame rate of the source video (312) and responsively adjusting the format of the resultant video signal (308).



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Format and Frame Rate Conversion for Display of 24Hz Source Video

This application is related to U.S. Patent Application Serial No. 09/001,952 (Attorney Docket No. 12713), filed on the same date as the present application.

This application is related to U.S. Patent Application Serial No. 09/001,620 (Attorney Docket No. 12669), filed on the same date as the present application.

The invention relates to video processing systems generally, and more particularly, video processing systems capable of receiving and processing a plurality of video signal formats, such as the various high definition and standard definition formats.

BACKGROUND OF THE DISCLOSURE

Present television receivers, such as NTSC (National Television Standards Committee) television receivers, include video processing circuitry that typically must process a video signal conforming to only a single, predetermined video format. Future digital television (DTV) receivers are expected to be implemented substantially in accordance with the transmission standards established by the Advanced Television Standards Committee (ATSC). A similar standard is the European Digital Video Broadcasting (DVB) standard. A compressed digital video system is described in the ATSC digital television standard document A/53, incorporated herein by reference. Moreover, the Moving Pictures Experts Group (MPEG) has promulgated several standards relating to digital data delivery systems. The first, known as MPEG-1, refers to ISO/IEC standards 11172 and is incorporated herein by reference. The second, known as MPEG-2, refers to ISO/IEC standards 13818 and is incorporated herein by reference. The new DTV standards allow broadcasters to deliver virtually any format up to 1920 x 1080 pixels. Specifically, DTV receivers must be capable of receiving source video comprising image sequences that vary in spatial resolution (480 lines, 720 lines, or 1080 lines), in temporal resolution (60 fps, 30 fps, or 24 fps), and in scanning format (2:1 interlaced or progressive scan).

It is known in the computer industry to display multiple graphics formats on a so-called "multisync" display device. Specifically, a multisync display changes horizontal and/or vertical scanning frequencies in response to a change in graphics format. Such a multisync approach may be implemented in a video or television environment by using, e.g., studio equipment raster formats standardized by the Society of Motion Picture and Television Engineers (SMPTE). Unfortunately, the multisync approach leads to an increase in cost due to the more complicated deflection circuitry, an increase in power consumption, and a high inter-format switching latency (i.e., greater than one video frame) due to long time constants associated with deflection coil inductance.

A better approach was disclosed by Lee in U.S. Patent No. 5,485,216, issued January 16, 1996 for Video Conversion Apparatus for High Definition Television, incorporated herein by reference in its entirety. In the Lee patent, a high definition television signal is decoded, then converted to a 30Hz frame rate, then vertically decimated, then horizontally decimated and then interleaved to produce a 30Hz, 1050 vertical scanning line video signal. Thus, the Lee arrangement provides a brute force technique for converting a high definition television signal into a 30Hz, 1050 vertical scanning line video signal. The format-converted television signal is then processed in a conventional manner to produce a picture.

Unfortunately, the Lee arrangement disadvantageously requires complex timing, switching and video processing circuitry. In addition, the television signal produced by the Lee arrangement will inherently cause motion video artifacts on a display device in the case of 24Hz source video (e.g., such as film). This is because the Lee arrangement uses the well known 3:2 pull-up sequence to convert 24 frames per second video into 60 frames per second, which results in motion jitter artifacts when the converted video is displayed. Since most prime time television is mastered on film, a large percentage of video material will be continue to be transmitted in one of the 24 Hz progressive scan formats.

Therefore, a need exists in the art for a cost-effective video processing system suitable for use in, e.g., a multiple format television receiver. It is also

seen to be desirable to provide a video processing system that adapts to use of 24Hz source video.

SUMMARY OF THE INVENTION

The invention is a method and concomitant apparatus for electronic format and frame rate conversion in a multiple format video processing system adapted to avoid display motion artifacts causes by 3:2 conversion of 24Hz video source video by tripling the frame rate of the source video and responsively adjusting the format of the resultant video signal.

Specifically, the invention is a method for use in a video processing system comprising a format converter and a frame rate converter, the format converter adapting at least one of a vertical format and a horizontal format of an input video signal in response to a format control signal, the frame rate converter adapting a frame rate of the input video signal in response to a frame rate control signal, the method comprising the steps of: identifying a format and frame rate of the input video signal; adapting the format of the input video signal to a native display format; and in the case of the frame rate of the input video signal being a first value, illustratively approximately 24Hz, tripling the frame rate of the input video signal.

The invention is also an apparatus for processing an input video signal having one of a plurality of video formats to produce an output video signal, the apparatus comprising: a format converter, coupled to receive the input video signal, for adapting a vertical and horizontal format of the input video signal in response to a format control signal; a frame rate converter, coupled to the format converter, for adapting a frame rate of the input video signal in response to a frame rate control signal; and a controller, coupled to the format converter and the frame rate converter, for generating the format control signal and the frame rate control signal; wherein the controller, in the case of an input video signal having a frame rate of a first value, causing the frame rate converter to triple the input video frame rate, and causing the format converter to adapt the vertical and horizontal format of the input video signal to a format suitable for use by the display device.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 shows high-level block diagram of a DTV receiver according to the invention;

FIG. 2 shows high-level block diagram of a DTV receiver according to the invention and including a light valve display; and

FIG. 3 is a flow diagram of a method for processing a video signal according to the invention.

DETAILED DESCRIPTION

The invention claims benefit of U.S. Provisional Application Number 60/060112, filed September 26, 1997, and incorporated herein by reference in its entirety.

The invention will be described within the context of a digital television (DTV) receiver, illustratively an ATSC television receiver. However, it will be apparent to those skilled in the art that the invention is applicable to any multiple format video processing system, including those systems adapted to DVB, MPEG-1, MPEG-2 and other information streams.

FIG. 1 shows high-level block diagram of a DTV receiver 100 according to the invention. Specifically, the DTV receiver 100 comprises a video processing section and a timing section. The video processing section comprises a video decoder 120, an optional de-interlacer 130, a vertical resizer 140, a horizontal resizer 150 and a frame buffer 160. The timing section comprises a clock circuit 110, a raster generator 190, a display clock 195, a read address generator 180 and a write address generator 185. A video signal S2 to be processed by the video processing section is received by, e.g., a DTV front end comprising, e.g., an antenna 102, a tuner 104, a demodulator 106 and a transport demultiplexer 108. A processed video signal S8 is displayed (after appropriate color matrix

processing) on, e.g., a display device 175 according to horizontal and vertical timing signals H-DEF and V-DEF that are produced by raster generator 190.

RF source 102 (illustratively, an antenna or cable television distribution network), provides a radio frequency (RF) signal RF comprising a plurality of television signals modulated according to a vestigial sideband (VSB), quadrature amplitude modulation (QAM) or other suitable modulation scheme. The provided RF television signals are coupled to tuner 104, which downconverts a desired television signal to produce a first intermediate frequency (IF) television signal IF. A demodulator 106, illustratively a VSB or QAM demodulator, demodulates the IF television signal IF to produce a digital information stream S1, illustratively an MPEG-like system stream S1 containing one or more MPEG-like program transport streams.

The MPEG-like program transport streams are analogous to NTSC channels, in that each program transport stream typically transports the video and audio portions of a single program, such as a movie or other audio-visual program. Each program transport stream comprises a plurality of elementary streams associated with the video and audio portions of the transported audio-visual program.

Transport demultiplexer 108 operates in a known manner to demultiplex a particular program transport stream from the MPEG-like system stream S1. Elementary audio stream(s) S3 associated with the demultiplexed program transport stream are coupled to an audio decoder 115 for decoding prior to processing by an audio driver circuit (not shown). Elementary video stream(s) S2 associated with the demultiplexed program transport stream are coupled to video decoder 120.

Transport demultiplexer 108 also extracts a program clock reference (PCR) signal included in so-called adaptation fields of selected transport stream packets (i.e., reference packets) of the demultiplexed program transport stream. The PCR is a sample of the 27MHz clock that was used to encode the demultiplexed program transport stream prior to transmission of the program transport stream. The extracted PCR is coupled to clock circuit 110.

Clock circuit 110 comprises, illustratively, a phase locked loop (PLL) 112, and a voltage controlled oscillator (VCO) 114. The clock circuit 110 generates a system clock f_{SYS}, illustratively a 27MHz system clock suitable for processing MPEG-like information streams. The clock circuit 110 utilizes the PCR extracted from the demultiplexed program transport stream to lock the decoder system clock (i.e., the system clock f_{SYS}) of DTV receiver 100 to the system clock of the encoder that produced demultiplexed program transport stream.

PLL 112 operates in a known manner to generate a control signal C1 in response to a comparison of the (nominally) 27MHz output of the VCO 114 to the PCR received from the transport demultiplexer 108. VCO 114, in response to control signal C1, operates in a known manner to increase or decrease the frequency of the 27MHz system clock f_{SYS}.

Video decoder 120 decodes the video stream S2 in a standard manner to produce a decoded video signal S4 having a given transmission format and frame rate. The video decoder 120 examines the sequence header of video stream S2 to determine the format, colorimetry (if available) and other information associated with the video signal encoded within video stream S2. Upon examining the sequence header, video decoder 140 couples the format, colorimetry and other information to an output as a header data signal HD.

Optional de-interlacer 130 receives the decoded video signal S4 and at least a portion of the header data signal HD. If the decoded video signal S4 comprises video information having an interlaced format (as indicated by the HD signal), then de-interlacer 130 converts the decoded video signal S4 into a progressive scan format video signal that is coupled to an output as video signal S5. If the decoded video signal S4 comprises video information having a progressive scan format, then de-interlacer 130 couples the decoded video signal S4 directly to the output as video signal S5. The de-interlacer 130 may be implemented, illustratively, using a motion-adaptive approach that requires frame(s) storage, or using a straightforward a vertical interpolation or line repetition approach.

Horizontal resizer 150 receives the video signal S5 and, in response to a control signal HS from controller 200, selectively changes the number of picture

elements (pixels) per line of video information included within video signal S5. Horizontal resizer 150 produces a horizontally resized video signal S6. Horizontal resizer 150 is capable of increasing the number of pixels per line by, e.g., using interpolation techniques to calculate luminance and chrominance information of a new pixel to be inserted between two existing pixels. Horizontal resizer 150 is capable of decreasing the number of pixels per line by, e.g., decimating a video line by removing every Nth pixel in the line.

Vertical resizer 140 receives the horizontally resized video signal S6 and, in response to a control signal VS from a controller 200, selectively changes the number of vertical scanning lines per frame of video information included within video signal S6. Vertical resizer 140 produces a vertically resized video signal S7. Vertical resizer 140 is capable of increasing the number of lines per video frame by, e.g., using interpolation techniques to calculate luminance and chrominance information of a new line to be inserted between two existing lines. Vertical resizer 140 is also capable of decreasing the number of lines per video frame by, e.g., decimating a video frame by using interpolation techniques to calculate new scan lines at a reduced line density.

In the case of optional de-interlacer 130 being implemented using the aforementioned vertical interpolation, or line repetition approach, the de-interlacing function may be incorporated within vertical resizing unit 140. In this case, horizontal resizer 150 is coupled to receive the decoded video signal S4 directly from the video decoder 120, as indicated by the dashed line in FIG. 1.

Frame buffer 160 receives the selectively vertically and horizontally resized video signal S7. Frame buffer 160 is a double buffering type of frame buffer comprising an input frame store buffer 162 and an output frame store buffer 164. The video information within video signal S7 is stored in the input frame store buffer 162 in response to a buffer input control signal IN. When the contents of the output frame store buffer 164 are entirely read, the contents of the input frame store buffer 162 are used as the output frame store buffer 164. That is, the input buffer and output buffer are functionally swapped, thereby obviating the need to transfer input buffer information into an output buffer. The video information stored in the output frame store buffer 164 is coupled to a

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frame buffer output as buffered video signal S8 in response to a buffer output control signal OUT. Since frame buffer 160 is a double buffering type of frame buffer, output data may be retrieved from the output frame store buffer 164 at data rate that is higher (or lower) than the rate at which input data is stored in the input frame store buffer 162. That is, the clock frequency associated with video signal S7 does not need to be the same as the clock frequency associated with buffered video signal S8. To utilize 30Hz video information for 60Hz display, each video frame is read out twice from the output frame store buffer 164 before the next video frame is move into the output frame store buffer 164..

Frame buffer 160 is, preferably, a double buffering arrangement as depicted in FIG. 1. It must be noted that a single buffering arrangement may also be used, but that the single buffer arrangement tends to produce a "tearing" artifact on a displayed image when the buffer read and buffer write rates are different. In the exemplary embodiment, the buffer read rate (determined by the OUT signal) and the buffer write rate (determined by the IN signal) are likely to be different, and, in the case of 24Hz source video, will be differed as will be described below. Such display rate conversion is required, since the direct use of a low transmission frame rate video signal (such as 24 or 30 Hz) would cause undesirable large area flicker for images displayed using most display technologies.

RGB matrix and driver 170 receives the buffered video signal S8. RGB matrix and driver 170 operates in a known manner to process buffered video signal S8 according to matrix coefficients, transfer characteristics and color primary information included within a sequence header of elementary video stream S2. Specifically, RGB matrix and driver 170 performs the color conversion processing needed to convert the transmitted Y, Cr, Cb color components to the red (R), green (G) and blue (B) color signals needed for display. The three color signals R, G, and B are coupled to a display device 175, where each color signal is used to drive, e.g., an associated electron gun in a picture tube (not shown). It must be noted that the three color signals R, G, and B generated by RGB matrix and driver 170 may require additional amplification

by appropriate driver circuitry (not shown) before being coupled to the display device 175.

Raster generator 190 generates a fixed frequency horizontal deflection signal H-DEF and a vertical deflection signal V-DEF in a conventional manner in response to a raster clock signal f_{RAST}. The raster clock signal f_{RAST} is generated in a conventional manner by a display clock circuit 195. The horizontal and vertical deflection signals H-DEF, V-DEF are used to drive, e.g., associated horizontal and vertical deflection coils, respectively, in a picture tube. It must be noted that the horizontal and vertical deflection signals H-DEF, V-DEF generated by raster generator 190 may require amplification by appropriate driver circuitry (not shown) before being coupled to the display device 175.

Write address generator 180 generates the frame buffer input control signal IN in response to a control signal WRITE, from controller 200, and the clock signal f_{SYS}. Similarly, read address generator 185 generates the buffer output control signal OUT in response to a control signal READ, from controller 200, and a clock signal f_{RAST}. It is important to note that the video information within video signal S7 is stored in the input frame store buffer 162 at a rate determined by a system clock f_{SYS}. Similarly, the video information stored in the output frame store buffer 164 is retrieved at a rate determined by a raster clock f_{RAST}. Thus, in the case of, e.g., a 27MHz display clock (e.g., optionally related to the 27MHz system clock f_{SYS}) and 81MHz raster clock f_{RAST}, data is retrieved from the frame buffer 160 at three times the storage rate.

Controller 200 may be implemented in a standard manner using a standard microprocessor, a memory unit comprising, and input/output port and associated support circuitry. Controller 200 may also comprise a special purpose digital signal processing circuit. Controller 200 receives format, colorimetry and other information relating to the decoded video signal S4 from the video decoder 120 via the header data signal HD. Controller 200 utilizes this information, and additional information related to the display device 175 (e.g., the native format of the display device), to generate a vertical size control signal VS for vertical resizer 140, a horizontal size control signal HS for horizontal resizer 150, a write

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address control signal WRITE for write address generator 180 and a read address control signal READ for read address generator 185

In one embodiment of the invention, all of the above processing and storage operations are performed using the 4:2:0 sampling (i.e., MPEG YUV) component format in order to minimize processing and storage requirements.

An ATSC receiver, such as the exemplary DTV receiver 100 of FIG. 1, will need to process video signals according to at least the ATSC recommended compression formats. These formats are shown below in Table 1. In Table 1, "P" denotes progressive scan and "I" denotes interlaced scan. It should also be noted that the frame rate numbers shown in Table 1 are integer values; the ATSC standard also allows the frame rate values to be multiplied by 1000/1001 (i.e., 59.94Hz, instead of 670Hz based).

Vertical lines	Pixels	Aspect ratio	Picture rate
1080	1920	16:9	60I, 30P, 24P
720	1280	16:9	60P, 30P, 24P
480	704	16:9 and 4:3	60P, 60I, 30P, 24P
480	640	4:3	60P, 60I, 30P, 24P

Table 1

In the DTV receiver 100 of FIG. 1, the normally independent video format conversion and display rate conversion processes are controlled and coordinated according to the invention. That is, the video format of an input video signal is controlled using the de-interlacer 130, the vertical resizer 140 and the horizontal resizer 150. Similarly, the display rate conversion process is controlled using the write address generator 180 and the read address generator 185. The controller 200 controls both processes, and coordinates the use of the processes to ensure that the image displayed on the display device 175 does not include motion artifacts caused by the use of 24Hz source material in 60Hz display devices.

Thus, in one embodiment of the DTV receiver 100 of FIG. 1, the display device 175 operates at a frame refresh rate of 60Hz (or 59.94Hz), with a

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type of projection display. As such, the DTV receiver 200 of FIG. 2 does not include circuitry for generating horizontal and vertical deflection signals. In this embodiment, the read address generator 185 is switched to a 6/5 (i.e., 72/60) higher frequency to provide a 72 Hz readout of the double buffered frame display when 24 Hz transmission formats are present. It should be noted that spatial format adjustments of 24Hz transmission formats are generally not required for such displays.

The following discussion will assume that the display device 175 comprises a cathode ray tube (CRT) display. In order to implement the invention in a cost-effective manner in CRT-based receivers, the horizontal deflection frequency of the CRT display should remain constant, thus requiring a 5/6 (i.e., 60/72) change in the number of scan lines. To change the number of scan lines, controller 200 causes vertical resizer 140 to reduce the number of lines in the video signal S5. To repeat a frame (i.e., 2:1 repeat), controller 200 causes the output frame store buffer 164 to be read twice before receiving the next frame. To repeat a frame twice (i.e., 3:1 repeat), controller 200 causes the output frame store buffer 164 to be read three times before receiving the next frame.

Table 2 shows a listing of video transmission and display formats, and processing parameters suitable for processing such video signals within the context of the DTV receiver 100. Specifically, the processing parameters are suitable for processing such video signals in the above-described manner for the case of display device 175 being a 1920 pixel by 1080 line progressive scan display having a horizontal scanning frequency of 64.8kHz. It should be noted that this display 175 is operated in a 900 line mode in the case of 24Hz source video.

The vertical interpolation parameter (Vert. Interp.), horizontal interpolation parameter (Horiz. Interp.) and frame repeat parameter (Frame Repeat) comprise, respectively, the vertical resizing factor, the horizontal resizing factor, and the frame rate conversion factor to be utilized by the controller 200 in response to a particular transmission format. The controller 200 modifies these parameters, as previously discussed, to preserve a fixed

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horizontal deflection frequency selected to implement one of the transmitted formats (the so-called native display format). Transmitted video information having a field or frame rate of 60Hz (or 59.94Hz) is not subjected to frame rate conversion. By contrast, transmitted video information having a frame rate 30Hz (or 29.97Hz) is converted to 60Hz (or 59.94Hz) using a 2:1 frame repeat. That is, the controller 200 causes the output frame store buffer 164 of frame buffer 160 to be read twice for each frame.

Since 24Hz frame rates cannot be displayed on a 60hz (or even 30Hz) display device without the undesirable motion artifacts due to the typical 3:2 frame rate conversion process, the DTV receiver 100 of FIG. 1 operates in a different manner when 24Hz video is decoded. Specifically, the 24Hz (or 24*1000/1001Hz) video is resized, as necessary in the format conversion process, and subsequently converted to 72Hz (or 72*1000/1001Hz) video in the frame rate conversion process. The display device 175 is operated at a 72Hz refresh rate when 24 Hz video is present. It must be noted that the format conversion process is adapted to the 72Hz frame rate conversion by the controller 200, as will be explained below.

Optionally, the 24Hz (or 24*1000/1001Hz) video is resized, as necessary in the format conversion process, and subsequently converted to 48Hz (or 48*1000/1001Hz) video in the frame rate conversion process. In the case of 48Hz operation, one skilled in the art using the teachings of this disclosure will be able to adapt the various parameters associated with implementing the described 72Hz method and apparatus to a 48Hz method and apparatus. Such 48Hz operation may be desirable where the display device is a liquid crystal display device. It is important to note that by utilizing an integer multiple (i.e., three for 72Hz and 2 for 48Hz), the invention avoids 3:2 artifacts as described herein.

FIG. 2 shows high-level block diagram of a DTV receiver according to the invention and including a light valve display. Since the DTV receiver 200 of FIG. 2 operates in substantially the same manner as the DTV receiver 100 of FIG. 1, only differences between the two figures will be discussed. Specifically, the DTV receiver 200 includes a display 175 comprising, illustratively, a light valve or digital micromirror display (DMD) type, or liquid crystal display (LCD)

horizontal display frequency and to avoid motion related artifacts in the case of 24Hz source video.

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Transmit Format	Trans. Rate	Display Format	Disp. Rate	De-Int ?	Vert. Interp.	Horiz. Interp.	Frame Repeat
1920x1080	60I	1920x1080	60P	yes	1	1	1:1
	30P	1920x1080	60P	no	1	1	2:1
	24P	**1920x900**	**72P**	**no**	**5/6**	**1**	**3:1**
1280x720	60P	1920x1080	60P	no	3/2	3/2	1:1
	30P	1920x1080	60P	no	3/2	3/2	2:1
	24P	**1920x900**	**72P**	**no**	**5/4**	**3/2**	**3:1**
704x480 (16:9)	60P	1920x1080	60P	no	9/4	30/11	1:1
	60I	1920x1080	60P	yes	9/4	30/11	1:1
	30P	1920x1080	60P	no	9/4	30/11	2:1
	24P	**1920x900**	**72P**	**no**	**15/8**	**30/11**	**3:1**
704x480	60P	1408x1080	60P	no	9/4	2/1	1:1
	60I	1408x1080	60P	yes	9/4	2/1	1:1
	30P	1408x1080	60P	no	9/4	2/1	2:1
	24P	**1408x900**	**72P**	**no**	**15/8**	2/1	**3:1**
640x480	60P	1920x1080	60P	no	9/4	2/1	1:1
	60I	1920x1080	60P	yes	9/4	2/1	1:1
	30P	1920x1080	60P	no	9/4	2/1	2:1
	24P	**1408x900**	72P	no	**15/8**	2/1	**3:1**

Table 2

Table 3 shows the same type of information as listed above in Table 2, except that Table 3 is directed to the case of display device 175 being a 1280 pixel by 720 line progressive scan display having a horizontal scanning frequency of 45kHz. It should be noted that this display is operated in a 600 line mode in the case of 24Hz source video.

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Transmit Format	Trans. Rate	Display Format	Disp. Rate	De-Int ?	Vert. Interp.	Horiz. Interp.	Frame Repeat
1920x1080	60I	1280x720	60P	yes	2/3	2/31	1:1
	30P	1280x720	60P	no	2/3	2/3	2:1
	24P	**1280x600**	**72P**	**no**	**5/9**	**2/3**	**3:1**
1280x720	60P	1280x720	60P	no	1	1	1:1
	30P	1280x720	60P	no	1	1	2:1
	24P	**1280x600**	**72P**	**no**	**5/6**	**1**	**3:1**
704x480 (16:9)	60P	1280x720	60P	no	3/2	20/11	1:1
	60I	1280x720	60P	yes	3/2	20/11	1:1
	30P	1280x720	60P	no	3/2	20/11	2:1
	24P	**1280x600**	**72P**	**no**	**5/4**	**20/11**	**3:1**
704x480	60P	960x720	60P	no	3/2	15/11	1:1
	60I	960x720	60P	yes	3/2	15/11	1:1
	30P	960x720	60P	no	3/2	15/11	2:1
	24P	**960x600**	**72P**	**no**	**5/4**	**15/11**	**3:1**
640x480	60P	960x720	60P	no	3/2	3/2	1:1
	60I	960x720	60P	yes	3/2	3/2	1:1
	30P	960x720	60P	no	3/2	3/2	2:1
	24P	**960x600**	**72P**	no	**5/4**	**3/2**	**3:1**

Table 3

Table 4 shows the same type of information as listed above in Tables 2-3, except that Table 4 is directed to the case of display device 175 being a 1920 pixel by 1080 line interlaced scan display having a horizontal scanning frequency of 32kHz. It should be noted that this display is operated in a 900 line mode in the case of 24Hz source video. The above approach for 1920x1080 progressive scan (Table 2) is used, but with modifications appropriate to the fact that the display is interlaced.

In this case, the complexity and memory required to implement the de-interlacer 130 can be substantially reduced, since the highest rate de-interlacing needs only be performed on 480 line format video. It should also be noted that the read address generation circuitry must be modified such that the double frame buffer 160 is capable of producing an interlaced scan format output signal S8.

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Transmit Format	Trans. Rate	Display Format	Disp. Rate	De-Int ?	Vert. Interp.	Horiz. Interp.	Frame Repeat
1920x1080	60I	1920x1080	60I	no	1	1	1:1
	30P	1920x1080	60I	no	1	1	2:1
	24P	**1920x900**	**72I**	**no**	**5/6**	**1**	**3:1**
1280x720	60P	1920x1080	60I	no	3/2	3/2	1:1
	30P	1920x1080	60I	no	3/2	3/2	2:1
	24P	**1920x900**	**72I**	**no**	**5/4**	**3/2**	**3:1**
704x480 (16:9)	60P	1920x1080	60I	no	9/4	30/11	1:1
	60I	1920x1080	60I	yes	9/4	30/11	1:1
	30P	1920x1080	60I	no	9/4	30/11	2:1
	24P	**1920x900**	**72I**	**no**	**15/8**	**30/11**	**3:1**
704x480	60P	1408x1080	60I	no	9/4	2/1	1:1
	60I	1408x1080	60I	yes	9/4	2/1	1:1
	30P	1408x1080	60I	no	9/4	2/1	2:1
	24P	**1408x900**	**72I**	**no**	**15/8**	2/1	**3:1**
640x480	60P	1920x1080	60I	no	9/4	2/1	1:1
	60I	1920x1080	60I	yes	9/4	2/1	1:1
	30P	1920x1080	60I	no	9/4	2/1	2:1
	24P	**1408x900**	**72I**	**no**	**15/8**	**2/1**	**3:1**

Table 4

Table 5 shows the same type of information as listed above in Tables 2-4, except that Table 5 is directed to the case of display device 175 being a 1280 pixel by 720 line interlaced scan display having a horizontal scanning frequency of 22.5kHz. It should be noted that this display is operated in a 600 line mode in the case of 24Hz source video. The above approach for 1280x720 progressive scan (Table 3) is used, but with modifications appropriate to the fact that the display is interlaced. Also, as noted above with respect to Table 4, the complexity and memory required in the de-interlacer 130 can be substantially reduced, and the read address generation circuitry 185 must be modified.

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Transmit Format	Trans. Rate	Display Format	Disp. Rate	De-Int ?	Vert. Interp.	Horiz. Interp.	Frame Repeat
1920x1080	60I	1280x720	60P	yes	2/3	2/31	1:1
	30P	1280x720	60P	no	2/3	2/3	2:1
	24P	**1280x600**	**72P**	**no**	**5/9**	**2/3**	**3:1**
1280x720	60P	1280x720	60P	no	1	1	1:1
	30P	1280x720	60P	no	1	1	2:1
	24P	**1280x600**	**72P**	**no**	**5/6**	**1**	**3:1**
704x480 (16:9)	60P	1280x720	60P	no	3/2	20/11	1:1
	60I	1280x720	60P	yes	3/2	20/11	1:1
	30P	1280x720	60P	no	3/2	20/11	2:1
	24P	**1280x600**	**72P**	**no**	**5/4**	**20/11**	**3:1**
704x480	60P	960x720	60P	no	3/2	15/11	1:1
	60I	960x720	60P	yes	3/2	15/11	1:1
	30P	960x720	60P	no	3/2	15/11	2:1
	24P	**960x600**	**72P**	**no**	**5/4**	**15/11**	**3:1**
640x480	60P	960x720	60P	no	3/2	3/2	1:1
	60I	960x720	60P	yes	3/2	3/2	1:1
	30P	960x720	60P	no	3/2	3/2	2:1
	24P	**960x600**	**72P**	no	**5/4**	**3/2**	**3:1**

Table 5

Tables 2-5 include several occurrences of interpolation ratios such as 30/11, 20/11 and 15/11. It should be noted that these ratios could be simplified to, respectively, 3/1, 2/1 and 3/2 in order to reduce interpolator complexity. Such simplification would, of course, result in some cropping of the active picture area.

FIG. 3 is a flow diagram of a method 300 for processing a video signal according to the invention. Specifically, FIG. 3 is a flow diagram of a method for optimally formatting a video signal such that a 3:2 pull-up artifact is not propagated through to a display device, such as the display device 175 depicted in FIGS. 1 and 2. The routine 300 of FIG. 3 may be implemented in hardware, software or a combination of hardware and software utilizing, illustratively, controller 200 of FIGS. 1 and 2.

The routine 300 of FIG. 3 is entered at step 302, when an input video signal is received by either the DTV receiver of FIG. 1, or the DTV receiver 200 of FIG. 2. At step 304 the format and frame rate of the video signal is identified, and the routine proceeds to step 306. At step 306 a query is made as to whether

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the format of the received video signal is compatible with the native format of the display device 175. If the query at step 306 is answered negatively, then the routine proceeds to step 308, where the format of the video signal is adapted to conform to the native format of the display device. The routine 300 then proceeds to step 310. If the query at step 306 is answered affirmatively, then the routine 300 proceeds to step 310.

At step 310 a query is made as to whether the frame rate of the received video signal is equal to approximately 24 Hz (e.g., 24 Hz or 23.97 Hz). If the query at step 310 is answered negatively, then the routine 300 proceeds to step 312, where the frame rate of the received video signal is tripled. That is, at step 312 the controller 200 causes a frame rate converter to increase the approximately 24 Hz frame rate of the input video signal to approximately 72 Hz. In this manner 3:2 pull-up artifacts typically associated with converting a 24 frame per second video signal into, e.g., 30Hz or 60Hz frame rate video signals are avoided. The routine 300 then proceeds to step 314, where it is exited.

The above-described embodiments of the invention provide methods and apparatus that avoid display motion artifacts causes by 3:2 conversion of 24Hz video source video. There are other format related functions that may be used to optimize the operations of, e.g., a multiple video format DTV receiver. For example, a multiple format video signal processing system operating in conjunction with a display device timing system to produce synchronized video and timing signals suitable for use by a fixed horizontal scanning frequency display device is described in more detail in co-pending U.S. Patent application No. 09/001952 (Attorney Docket No. 12713) filed on the same day as the present application, and incorporated herein by reference in its entirety. Another example is a video processing system that automatically adjusts video processor operations, such as horizontal peaking, vertical peaking and colorimetry parameters, depending upon the format of a received video signal is described in more detail in co-pending U.S. Patent application
No. 09/001620 (Attorney Docket No. 12669), filed on the same day as the present application, and incorporated herein by reference in its entirety.

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Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

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What is claimed is:

1. Apparatus for processing an input video signal having one of a plurality of video formats to produce an output video signal, said apparatus comprising:

a format converter, coupled to receive said input video signal, for adapting a vertical and horizontal format of said input video signal in response to a format control signal;

a frame rate converter, coupled to said format converter, for adapting a frame rate of said input video signal in response to a frame rate control signal; and

a controller, coupled to said format converter and said frame rate converter, for generating said format control signal and said frame rate control signal;

said controller, in the case of an input video signal having a frame rate of a first value, causing said frame rate converter to multiply, by an integer value, said input video frame rate, and causing said format converter to adapt said vertical and horizontal format of said input video signal to a format suitable for use by said display device.

2. The apparatus of claim 1, wherein said first value is approximately 24Hz.

3. The apparatus of claim 1, wherein said integer value is two or three.

4. The apparatus of claim 2, wherein said integer value is two or three.

5. Apparatus for processing an input video signal having one of a plurality of video formats to produce an output video signal for use by one of a light valve, DMD or LCD display device, said apparatus comprising:

a frame rate converter, coupled to said format converter, for adapting a frame rate of said input video signal in response to a frame rate control signal; and

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a controller, coupled to said format converter and said frame rate converter, for generating said format control signal and said frame rate control signal;

said controller, in the case of an input video signal having a frame rate of a first value, causing said frame rate converter to multiply, by an integer value, said input video frame rate.

6. The apparatus of claim 5, wherein said first value is approximately 24.

7. The apparatus of claim 5, wherein said integer value is two or three.

8. Method for use in a video processing system, said video processing system comprising a format converter and a frame rate converter, said format converter adapting at least one of a vertical format and a horizontal format of an input video signal in response to a format control signal, said frame rate converter adapting a frame rate of said input video signal in response to a frame rate control signal, said method comprising the steps of:

identifying a format and frame rate of said input video signal;

adapting said format of said input video signal to a native display format; and

in the case of said frame rate of said input video signal being a first value, multiplying, by an integer value, said frame rate of said input video signal.

9. The method of claim 8, wherein said first value is approximately 24Hz.

10. The method of claim 9, wherein said integer value is two or three.

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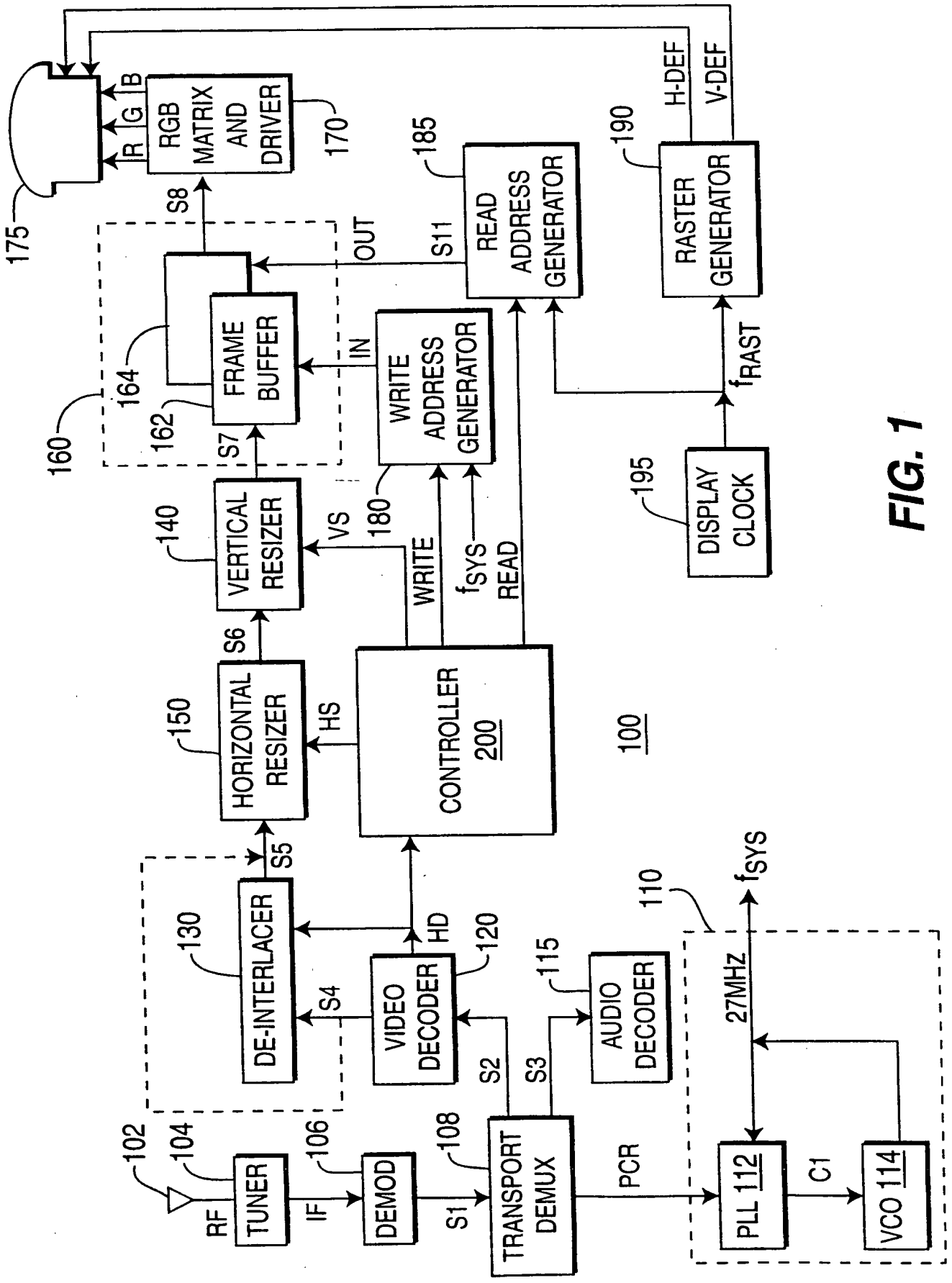

FIG. 1

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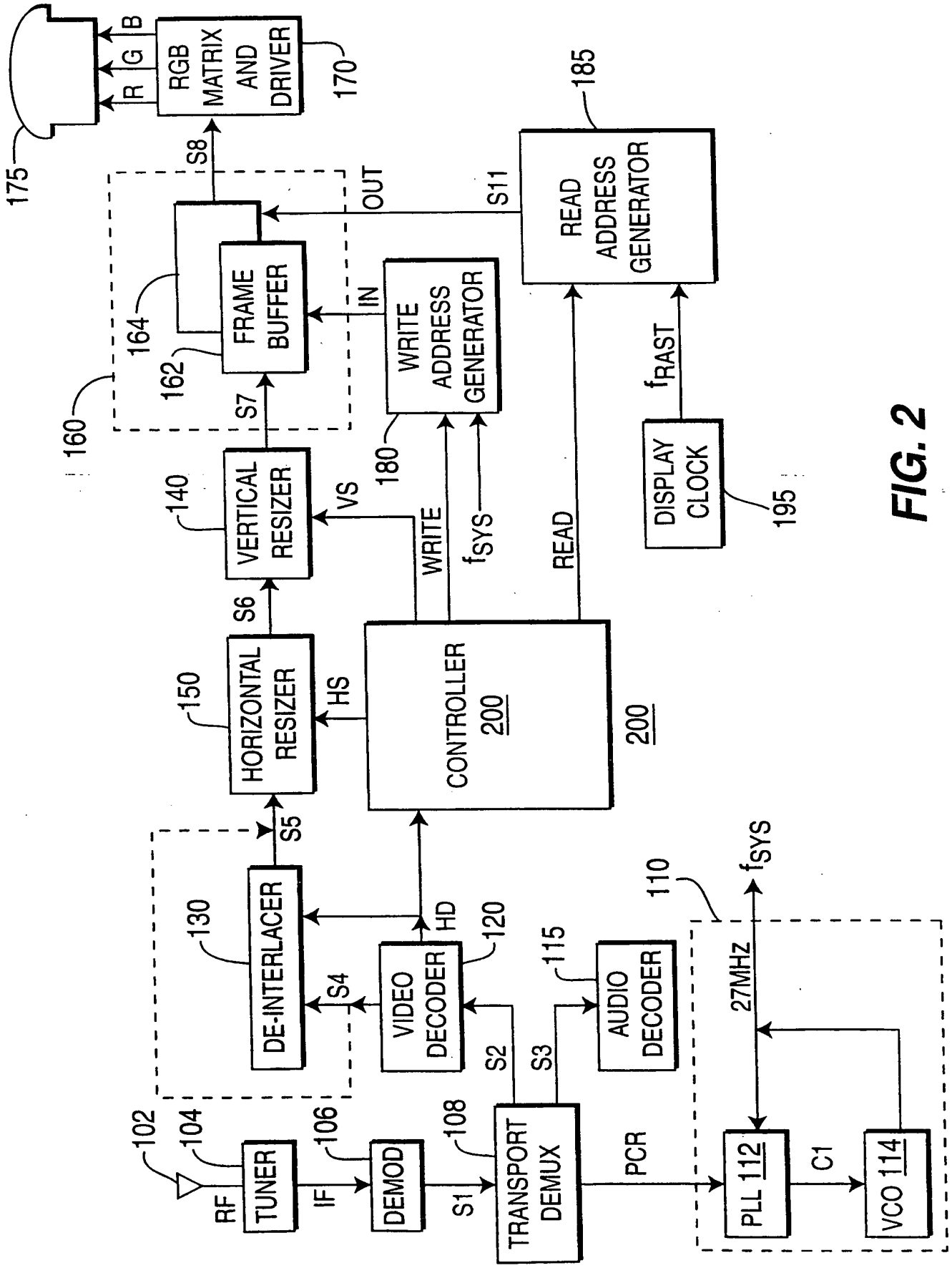

FIG. 2

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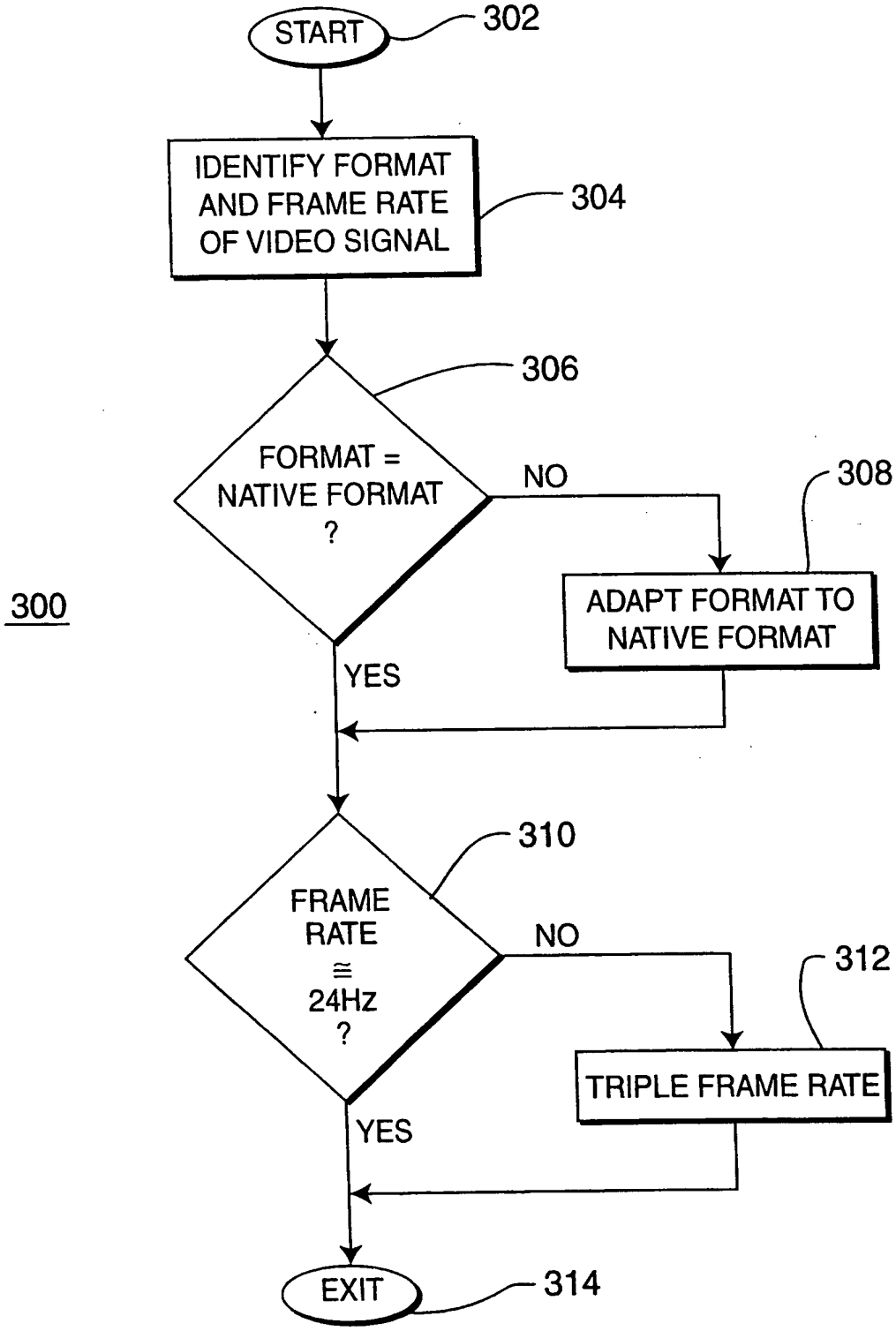

FIG. 3

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/27542

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04N 7/01
US CL : 348/441
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/441, 443, 447, 448, 459, 458

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: digital micromirror display, liquid crystal display

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,485,216 A (LEE) 16 January 1996, Column 4, lines 53-67; column 2, lines 1-4; column 5, lines 26-42.	1,2,8 and 9
Y		3-7 and 10
Y	EP 0 600 446 A2 (IKUO) 08 June 1994, column 20, lines 44-52.	3,4,7 and 10
Y	US 5,452,024 A (SAMPSELL) 19 September 1995, Column 2, lines 54-68.	5-7

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 03 MARCH 1999	Date of mailing of the international search report 23 APR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ALEXANDER BERHE Fanna R. Matthews Telephone No. (703) 305-2429

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